WE CLAIM:

1. A substrate for use in semiconductor devices, said substrate having first and second surfaces, comprising:
   a base structure comprising insulating material;
   a plurality of I/O terminal pads distributed on at least one of said first and second surfaces, said terminal pads interconnected by conducting traces;
   a plurality of selected metal layers distributed in said base structure, said metal layers substantially parallel to said surfaces, separated by said insulating material from each other and from said surfaces; and
   at least one metal layer opposite said at least one of said surfaces having annular openings therein configured so that metal areas within said openings directly opposite each of said terminal pads are electrically isolated from the remainder of said layer.
2. The substrate according to Claim 1 wherein the width of said openings is selected to provide a pre-determined capacitance between each of said terminal pads and the remainder of said metal layer.
3. The substrate according to Claim 1 wherein said layers include power supply layers and layers at ground potential.
4. The substrate according to Claim 3 wherein said layers opposite each of said surfaces are at ground potential.
5. The substrate according to Claim 1 wherein said metal areas have approximately the same size as said terminal pads.

6. The substrate according to Claim 1 wherein said openings have circular or rectangular outlines.

7. The substrate according to Claim 1 wherein each of said isolated metal areas is connected to a via and thereby mechanically anchored by said via.

8. The substrate according to Claim 1 wherein said selected metal layers in said base structure, from one of said surfaces to the center of said base structure, provide the configuration of an annular opening surrounding an electrically isolated portion of the respective layer, aligned with said respective terminal pad.

9. The substrate according to Claim 1 wherein said capacitance is determined as the series sum of the capacitive contributions from said isolated area and said opening.

10. The substrate according to Claim 1 wherein said insulating material is a ceramic.

11. The substrate according to Claim 1 wherein said insulating material is a polymer.

12. A semiconductor device comprising:

an integrated circuit chip having contact pads;

a substrate, having first and second surfaces, said substrate comprising insulating material, said substrate having a plurality of I/O terminal pads distributed on at least one of said first and second surfaces, said terminal pads interconnected by conducting traces;

a plurality of selected metal layers distributed in said substrate, substantially parallel to said surfaces, separated by said insulating material from each other and from said surfaces;

at least one metal layer opposite each of said at least one of said surfaces having annular openings therein configured so that metal areas within said openings directly opposite each of said terminal pads are isolated from the remainder of said metal layer; and

said chip contact pads connected to said plurality of substrate terminal pads on said first surface.

13. The device according to Claim 12 wherein said chip pads are connected to said substrate terminal pads by reflow interconnections.

14. The device according to Claim 12 wherein said chip pads are connected to said substrate terminal pads by bonding wires.

15. The device according to Claim 12 wherein reflow interconnection elements are attached to said I/O terminal pads on said second substrate surface.

16. A method to fabricate a substrate for use in semiconductor devices, comprising the steps of:

providing a base structure having first and second surfaces, said base structure comprising insulating material;

forming a plurality of I/O terminals distributed on at least one of said first and second surfaces, said terminal pads interconnected by conducting traces;

forming a plurality of selected metal layers distributed in said base structure, said metal layers substantially parallel to said surfaces, separated by said insulating material from each other and from said surfaces; and

forming at least one metal layer opposite said at least one of said surfaces to provide annular openings

therein and configure said openings so that metal areas within said openings are directly opposite each of said terminal pads, electrically isolated from the remainder of said layer.

17. The method according to Claim 16 wherein the width of said openings is selected to provide a pre-determined capacitance between each of said terminal pads and the remainder of said metal layer.

18. The method according to Claim 17 wherein said capacitance is determined as the series sum of the capacitive contributions from said isolated area and said opening.

19. The method according to Claim 16 wherein said metal areas have approximately the same size as said terminal pads.

20. The method according to Claim 16 wherein said insulating material is a ceramic.

21. The method according to Claim 16 wherein said insulating material is a polymer.